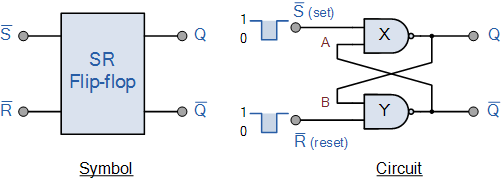
**LAB EXPERIMENT 4**

**Aim:** To design SR Flip flop and JK Flip flop in XILINX software and check the outputs in the simulation.

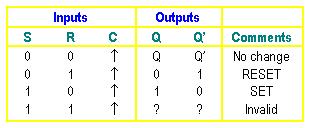
**Theory:**

1. SR Flip Flop: In this circuit when you Set “S” as active the output “Q” would be high and “Q‘‘” will be low. Once the outputs are established, the wiring of the circuit is maintained until “S” or “R” go high, or power is turned off.

Circuit Diagram:

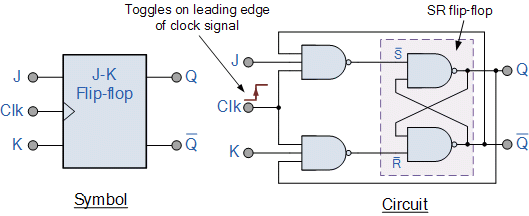


Truth Table:

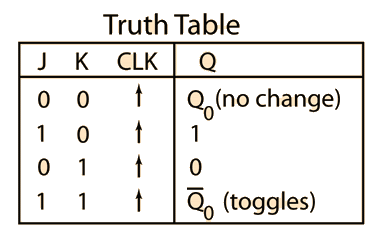


1. JK Flip Flop: The JK flip flop is an improvement on the SR flip flop where S=R=1 is not a problem. The input condition of J=K=1, gives an output inverting the output state. However, the outputs are the same when one tests the circuit practically.

Circuit Diagram:



Truth Table:



**Verilog Code of the Program and Outputs:**

1. **SR Flip Flop:**
2. **Verilog Code:**

module srff\_Rahil(q,qbar,s,r,clk);

input s,r,clk;

output q,qbar;

wire nand1\_out;

wire nand2\_out;

nand(nand1\_out,clk,s);

nand(nand2\_out,clk,r);

nand(q,nand1\_out,qbar);

nand(qbar,nand2\_out,q);

endmodule

1. **Screenshots of the Program and Outputs:**

Graphical user interface, text, application

Description automatically generated

Graphical user interface

Description automatically generated

1. **RTL Schematics:**

A picture containing text, indoor, monitor, screenshot

Description automatically generated

Graphical user interface

Description automatically generated

**Conclusion:** From this experiment we have learnt how to design SR and JK Flip Flop in Xilinx Software.